AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-20. (canceled).

21. (previously presented): A differential amplifier circuit comprising:

a differential stage including:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a first power supply; and

a current source connected between said differential pair and a second power supply and supplying a current to said differential pair;

said differential pair and/or said load element pair comprised of transistors each having relatively low threshold value; and

a switch circuit inserted in a current path of said differential stage for controlling an activation and deactivation of said differential stage, said switch circuit comprising at least one transistor which has a threshold value higher than that of the transistors having relatively low threshold value and which is controlled to be on and off by a control signal supplied to a control terminal thereof.

22. (currently amended): The differential amplifier circuit according to claim 40, wherein said switch circuit comprises said transistor having said relatively high absolute value of the second threshold value connected in series with said current source between said differential pair and said second power supply~~, said transistor having the absolute value of the threshold value higher than said relatively low absolute value of the threshold value of said transistor~~ and comprising the control terminal for receiving said control signal to be controlled to be on and off; ~~or:~~

~~said switch circuit comprises said current source comprised of said transistor having the absolute value of the threshold value higher than said relatively low absolute value of the threshold value of said transistor and including the control terminal for receiving a bias signal as said control signal to be controlled to be on and off.~~

23. (currently amended): The differential amplifier circuit according to claim 40, wherein said switch circuit comprises said transistor, having said relatively high absolute value of said second threshold value~~, the absolute value of the threshold value higher than said relatively low absolute value of the threshold value of said transistor~~ and including the control terminal for receiving said control signal to be controlled to be on and off for activating and inactivating said load element pair.

24. (currently amended): A differential amplifier circuit comprising:

a differential stage comprising:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a first power supply; and

a current source connected between said differential pair and a second power supply and supplying a current to said differential pair;

an output amplification stage receiving an output of said differential stage and having an output terminal for outputting an output signal, said output amplification stage comprising an output stage transistor connected between said output terminal and said first power supply;

said differential pair and/or said load element pair including at least a transistor which has relatively low absolute value of a first threshold value;

a first switch circuit for controlling an activation and deactivation of said differential stage, wherein said first switch circuit comprises a transistor connected in series with said current source between said differential pair and said second power supply, having ~~an~~ a relatively high absolute value of a second threshold value higher than said relatively low absolute value of the first threshold value ~~of said transistor~~ and comprising a control terminal for receiving a control signal to be controlled to be on and off, or said first switch circuit comprises said current source comprised of a transistor having an-a relatively high absolute value of a third threshold value higher than said relatively low absolute value of the first threshold value ~~of said transistor~~ and including a control terminal for receiving a control signal to be controlled to be on and off; and

a second switch circuit for controlling an activation and deactivation of said output amplification stage, comprising a transistor connected between the control terminal of said output stage transistor and one of said first and second power supplies, having ~~an~~ a relatively high absolute value of a fourth threshold value higher than said relatively low absolute value of the first threshold value ~~of said transistor~~ and comprising a control terminal for being controlled by said control signal to be on and off complementarily with the transistor constituting said first switch circuit.

25. (currently amended): A differential amplifier circuit comprising:

a differential stage including:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a first power supply, said load element pair comprised of a transistor pair, conductivity type of which is opposite that of a transistor pair composing said differential pair; and

a current source connected between said differential pair and a second power supply and supplying a current to said differential pair;

an output amplification stage receiving an output of said differential stage and having an output terminal for outputting an output signal, said output amplification stage comprising an output stage transistor connected between said output terminal and said first power supply;

said differential pair, and/or, said load element pair including at least a transistor which has relatively low absolute value of a first threshold value;

a first switch circuit for controlling an activation and deactivation of said differential stage, wherein said first switch circuit comprises a transistor connected in series with said current source between said differential pair and said second power supply, having an-a relatively high absolute value of a second threshold value higher than said relatively low absolute value of the first threshold value of said transistor and including a control terminal for receiving a control signal to be controlled to be on and off, or said first switch circuit comprises said current source comprised of a transistor having ~~an~~ a relatively high absolute value of a third threshold value higher than said relatively low absolute value of the first threshold value ~~of said transistor~~ and comprising a control terminal for receiving a control signal to be controlled to be on and off;

a transistor connected in series with said output stage transistor between said output terminal and said first power supply, having ~~an~~ a relatively high absolute value of a fourth threshold value higher than said relatively low absolute value of the first threshold value of said transistor and comprising a control terminal for being controlled by said control signal to be on and off in phase with said transistor constituting said first switch circuit.

26. (currently amended): The differential amplifier circuit according to claim 24, further comprising a transistor connected between said output terminal and said second power supply, having ~~an~~ a relatively high absolute value ~~a threshold value~~ of a fifth threshold value higher than

said relatively low absolute value of the first threshold value ~~of said transistor~~ and comprising a control terminal for being controlled to be on and off by said control signal.

27. (previously presented): The differential amplifier circuit according to claim 24, wherein a conductivity type of said output stage transistor is opposite that of said differential pair.

28. (currently amended): The differential amplifier circuit according to claim 24, wherein ~~said~~ another output amplification stage further comprises a transistor connected in series with said current source between said output terminal and said second power supply, having ~~an~~ a relatively high absolute value of a fifth threshold value higher than said relatively low absolute value of the threshold value of said transistor and comprising a control terminal for being controlled to be on and off by said control signal.

29. (currently amended): A differential amplifier circuit comprising:

first and second input terminals;

an output terminal;

a first differential stage comprising:

a first differential pair for differentially receiving signal voltages supplied to said first and second input terminals;

a first load element pair connected between an output pair of said first differential pair and a first power supply, said first load element pair comprised of a transistor pair, a

conductivity type of ~~which~~ the transistor pair of said first load element pair is opposite that of a transistor pair composing said first differential pair; and

a first current source connected between said first differential pair and a second power supply and supplying a current to said first differential pair;

a second differential stage comprising:

a second differential pair for differentially receiving signal voltages supplied to said first and second input terminals, said second differential pair comprised of a transistor pair, a conductivity type of ~~which~~ the transistor pair of said second differential pair is opposite that of the transistor pair composing said first differential pair;

a second load element pair connected between an output pair of said second differential pair and said second power supply, said second load element pair comprised of a the transistor pair, a conductivity type of which the transistor pair of said second load element is opposite that of a transistor pair composing said second differential pair; and

a second current source connected between said second differential pair and said first power supply and supplying a current to said second differential pair;

a first output amplification stage receiving an output of said first differential pair and outputting an output signal from said output terminal;

a second output amplification stage receiving an output of said second differential pair and outputting an output signal from said output terminal;

said first differential pair and/or said first load element pair being comprised of transistors each having relatively low absolute value of a first threshold value; and

said second differential pair and/or said second load element pair comprised of transistors each having relatively low absolute value of a second threshold value;

a first switch circuit for controlling an activation and deactivation of said first differential stage, wherein said first switch circuit comprises a transistor connected in series with said first current source between said first differential pair and said second power supply, having ~~an~~ a relatively high absolute value of a third threshold value higher than said relatively low absolute value of the first threshold value of said transistors and comprising a control terminal for receiving a first control signal for being controlled to be on and off, or said first switch circuit comprises said first current source comprised of a transistor having ~~an~~ a relatively high absolute value of a fourth threshold value higher than said relatively low absolute value of the first threshold value of said transistors and comprising a control terminal for receiving a first bias voltage as said first control signal to be controlled to be on and off; and

a second switch circuit for controlling an activation and deactivation of said second differential stage; wherein said second switch circuit comprises a transistor connected in series with said second current source between said second differential pair and said first power supply, having ~~an~~ a relatively high absolute value of a fifth threshold value higher than said relatively low absolute value of the second threshold value ~~of said transistors~~ and comprising a control terminal for receiving a second control signal for being controlled to be on and off, or said second switch circuit comprises said second current source comprised of a transistor having ~~an~~ a relatively high absolute value of a sixth threshold value higher than said relatively low absolute

value of the second threshold value ~~of said transistors~~ and comprising a control terminal for receiving a second bias voltage as said second control signal to be controlled to be on and off.

30. (currently amended): The differential amplifier circuit according to claim 29, wherein:

said first output amplification stage comprises a first output stage transistor having relatively low absolute value of a ~~third~~ seventh threshold value connected between said output terminal and said first power supply;

said second output amplification stage includes a second output stage transistor having a relatively low absolute value of a ~~fourth~~ eighth threshold value, connected between said output terminal and said second power supply; and

said differential amplifier circuit further comprises:

a third switch circuit for controlling activation and deactivation of said first output amplification stage, comprising a transistor connected in series with said first output stage transistor between said output terminal and said first power supply, having a control terminal for being controlled by said first control signal to be on and off in phase with on and off of said first switch circuit, and having ~~an~~ a relatively high absolute value of a ninth threshold value higher than said relatively low absolute value of the ~~third~~ seventh threshold value ~~of said transistors~~; and

a fourth switch circuit for controlling activation and deactivation of said second output amplification stage, comprising a transistor connected in series with said second output stage transistor between said output terminal and said second power supply, having a control

terminal for being controlled by said second control signal to be on and off in phase with on and off of said second switch circuit, and having ~~an~~ a relatively high absolute value of a tenth threshold value higher than said relatively low absolute value of the ~~fourth~~ eighth threshold value ~~of said transistors~~.

31. (currently amended): The differential amplifier circuit according to claim 30, wherein:

said first output amplification stage further comprises a transistor connected between said output terminal and said second power supply, having ~~an~~ a relatively high absolute value of a eleventh threshold value higher than said relatively low absolute value of the ~~third~~ seventh threshold value ~~of said transistor~~ and comprising a control terminal for being controlled by said first control signal to be on and off in phase with said first switch circuit; and wherein

said second output amplification stage further comprises a transistor connected between said output terminal and said first power supply, having ~~an~~ a relatively high absolute value of a twelfth threshold value higher than said relatively low absolute value of the ~~fourth~~ eighth threshold value ~~of said transistor~~ and comprising a control terminal for being controlled by said second control signal to be on and off in phase with said second switch circuit.

32. (previously presented): The differential amplifier circuit according to claim 29, wherein:

said first output amplification stage comprises a transistor, a conductivity of which is opposite that of said first differential pair; and

said second output amplification stage comprises a transistor, a conductivity of which is opposite that of said second differential pair.

33. (previously presented): The differential amplifier circuit according to claim 29, further comprising a circuit for controlling to charge and/or discharge of said output terminal at a predetermined timing before the output signal is output from said output terminal.

34. (currently amended): The differential amplifier circuit according to claim 30, wherein:

said first output amplification stage comprises a transistor connected in series with a current source between said output terminal and said second power supply, having ~~an~~ a relatively high absolute value of a eleventh threshold value higher than said relatively low absolute value of the ~~third~~ seventh threshold value ~~of said transistor~~ and comprising a control terminal for being controlled by said first control signal to be on and off in phase with said first switch circuit; and

said second output amplification stage comprises a transistor connected in series with a current source between said output terminal and said first power supply, having ~~an~~ a relatively high absolute value of a twelfth threshold value higher than said relatively low absolute value of the ~~fourth~~ eighth threshold value of ~~said transistor~~ and comprising a control terminal for being controlled by said first control signal to be on and off in phase with said second switch circuit.

35. (previously presented): A differential amplifier circuit comprising:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a power supply; and

a current source for supplying a current to said differential pair;

said differential pair, and/or, said load element pair being comprised of transistors each having relatively low threshold value;

wherein said current source is comprised of a transistor having a threshold value higher than that of the transistors having relatively low threshold value and comprising a control terminal for receiving a bias voltage as a control signal to be controlled to be on and off.

36. (currently amended): A differential amplifier circuit comprising:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a power supply; and

a current source for supplying a current to said differential pair;

said differential pair and/or said load element pair including at least a transistor which has relatively low absolute value of a first threshold value;

said differential amplifier circuit further comprising a switch circuit for controlling activation and deactivation of said differential amplifier circuit, wherein switch circuit comprises at least one transistor having ~~an~~ a relatively high absolute value of a second threshold value higher than said relatively low absolute value of the first threshold value of said transistor and comprising a control terminal for receiving a control signal to be controlled to be on and off.

37-39. (canceled).

40. (currently amended): A differential amplifier circuit comprising:

a differential stage including:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a first power supply; and

a current source connected between said differential pair and a second power supply and supplying a current to said differential pair;

said differential pair and/or said load element pair including at least a transistor which has ~~relatively low absolute value of a threshold value~~a relatively low absolute value of a first threshold value; and

a switch circuit inserted in a current path of said differential stage for controlling an activation and deactivation of said differential stage, said switch circuit comprising at least one

transistor which has ~~an absolute value of a threshold value higher than said relatively low absolute value of the threshold value of said transistor~~ a relatively high absolute value of a second threshold value higher than said relatively low absolute value of the first threshold value and which is controlled to be on and off by a control signal supplied to a control terminal thereof.

41. (canceled).

42. (currently amended): The differential amplifier circuit according to claim 40, wherein said transistor which has said relatively low absolute value of the first threshold value and said transistor which has said relatively high absolute value of the second threshold-value-higher-than ~~said relatively low absolute value of the threshold value of said transistor~~, are composed by a ~~thin film transistor~~ thin film transistors including a crystalline silicon film as an active layer formed on a insulating substrate.

43. (currently amended): The differential amplifier circuit according to claim 40, wherein said transistor which has said relatively low absolute value of the first threshold value and said transistor which has said relatively high absolute value of the second threshold value-higher-than ~~said low absolute value of the threshold value of said transistor~~, are composed by ~~a thin film transistor~~ thin film transistors including a polycrystalline silicon film as an active layer formed on an insulating substrate.

44-45. (canceled).

46. (previously presented): A memory device comprising a sense amplifier including the differential amplifier circuit as set forth in claim 40.

47. (canceled).

48. (currently amended): A semiconductor device including the differential amplifier circuit as set forth in claim 40, wherein said transistor which has said relatively low absolute value of the first threshold value and said transistor which has ~~said absolute value of the threshold value~~ said relatively high absolute value of the second threshold value~~higher than said low absolute value of the threshold value of said transistor~~, within the differential amplifier circuit being composed by a thin film transistors including a crystalline silicon film as an active layer on a insulating substrate.

49-52. (canceled).

53. (currently amended): The differential amplifier circuit according to claim 24, wherein said transistor which has said relatively low absolute value of the first threshold value and said transistors which have ~~said absolute value~~ said relatively high values of the ~~threshold value~~ second, third and fourth threshold values~~higher than said relatively low absolute value of the~~

~~threshold value of said transistor~~, are composed by ~~a~~ thin film transistors including a crystalline silicon film as an active layer on an insulating substrate.

54. (currently amended): The differential amplifier circuit according to claim 24, wherein said transistor which has said relatively low absolute value of the first threshold value and said transistors which have ~~said absolute value~~ said relatively high absolute values of the ~~threshold value~~ second, third and fourth threshold~~higher than said relatively low absolute value of the threshold value of said transistor~~, are composed by ~~a~~ thin film transistors including a polycrystalline silicon film as an active layer formed on an insulating substrate.

55. (currently amended): The differential amplifier circuit according to claim 25, wherein said transistor which has said relatively low absolute value of the first threshold value ~~and~~ and said transistors which have ~~said absolute value of said transistor,~~ said relatively high absolute values of the second, third and fourth threshold values are composed by ~~a~~ thin film transistors including a crystalline silicon film as an active layer on an insulating substrate.

56. (currently amended): The differential amplifier circuit according to claim 25, wherein said transistor which has said relatively low absolute value of the first threshold value and said transistors which have ~~said absolute value of the threshold value~~ said relatively high absolute values of the second, third and fourth threshold values ~~higher than said relatively low absolute~~

~~value of the threshold value of said transistor,~~ are composed by ~~a~~ thin film transistors including a polycrystalline silicon film as an active layer formed on an insulating substrate.

57. (currently amended): The differential amplifier circuit according to claim 29, wherein said transistors, which have said relatively low absolute values of the first and second threshold values and said transistors which have ~~absolute value of the threshold value~~ said relatively high absolute values of the third, fourth, fifth and sixth threshold values~~higher than said low absolute values of the first and second threshold values of said transistors~~, are composed by a thin film transistors including a crystalline silicon film as an active layer on an insulating substrate.

58. (currently amended): The differential amplifier circuit according to claim 29, wherein said transistors, which ~~have said relatively low absolute value of the first and second threshold value~~ said relatively low absolute values of the first and second threshold values and said transistors which have ~~said absolute value of the threshold value~~ said relatively high absolute values of the third, fourth, fifth and sixth threshold values~~higher than said relatively low absolute value of the first and second threshold value of said transistors~~, are composed by ~~a~~ thin film transistors including a polycrystalline silicon film as an active layer formed on an insulating substrate.

59. (currently amended): The differential amplifier circuit according to claim 63, wherein said transistor which has ~~said relatively low absolute value of the threshold value~~ said relatively

low absolute value of the first threshold value and said transistor which has ~~said absolute value of the threshold value~~ said relatively high absolute value of the second threshold value~~higher than said relatively low absolute value of the threshold value of said transistor~~, are composed by a-thin film transistors including a crystalline silicon film as an active layer on an insulating substrate.

60. (currently amended): The differential amplifier circuit according to claim 63, wherein said transistor which has said ~~relatively low absolute value of the threshold value~~ said relatively low absolute value of the first threshold value and said transistor which has ~~said absolute value of the threshold value~~ said relatively high absolute value of the second threshold~~higher than said relatively low absolute value of the threshold value of said transistor~~, are composed by a-thin film transistors including a polycrystalline silicon film as an active layer formed on an insulating substrate.

61. (currently amended): The differential amplifier circuit according to claim 36, wherein said transistor which has said relatively low absolute value of the first threshold value and said transistor which has ~~said absolute value of the threshold value higher that said relatively low absolute value of the threshold value of said transistor~~said relatively high absolute value of the second threshold value, are composed by a-thin film transistors including a crystalline silicon film as an active layer on an insulating substrate.

62. (currently amended): The differential amplifier circuit according to claim 36, wherein said transistor which has said relatively low absolute value of the first threshold value and said transistor which has ~~said absolute value of the threshold value higher than said relatively low absolute value of the threshold value of said transistor~~said relatively high absolute value of the second threshold value, ~~is~~ are composed by ~~a~~ thin film transistors including a polycrystalline silicon film as an active layer formed on a insulating substrate.

63. (currently amended): A differential amplifier circuit comprising:

a differential pair for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair connected between an output pair of the differential pair and a power supply; and

a current source for supplying a current to said differential pair;

said differential pair; and/or said load element pair including at least a transistor which has relatively low absolute value of a first threshold value;

wherein said current source is comprised of a transistor having ~~an absolute value of a threshold value~~ a relatively high absolute value of a second threshold value higher than ~~said low absolute value of the threshold value~~ said low relatively low absolute value of the first threshold

value ~~of the transistor~~ and comprising a control terminal for receiving a bias voltage as a control signal to be controlled to be on and off.

64. (new): A data driver comprising the differential amplifier circuit according to claim 40.

65. (new): A display unit comprising the differential amplifier circuit according to claim 40.

66. (new): A thin semiconductor unit comprising a differential amplifier circuit according to claim 40.